

CLAIMS

What is claimed is:

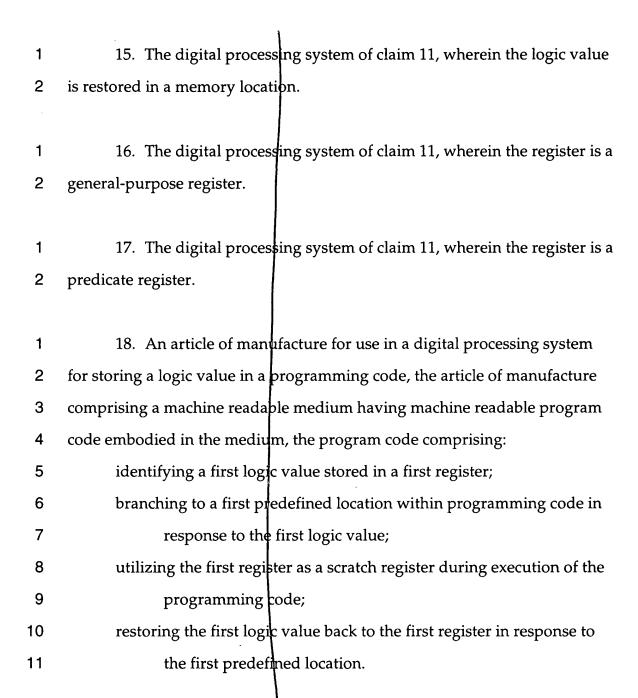
1. A method for	restoring a memory value comprising:
identifying a first	logic value stored in a first register;
branching to a fir	st predefined location within programming code
based upo	n the first logic value;
utilizing the first	register as a scratch register during execution of the
programm	aing code;
restoring the first	logic value back to the first register after execution
of the pro	gramming code has finished.
2. The method	of claim 1 further comprising detecting an occurrence
of an interrupt during e	xecution.

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1	3. The method of claim 1 further comprising:
2	identifying a second logic value stored in a second register;
3	branching to a second predefined location within the programming
4	code based upon the second logic value;
5	utilizing the second register as scratch register during execution of the
6	programming code;
7	restoring the second logic value back to the second register in
8	response to the second predefined location.
1	5. The method of claim 1, wherein the branching to a first
2	predefined location further including identifying the first predefined location
3	from a plurality of predefined locations in the programming code.
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1	6. The method of claim 1 further comprising executing the
2	programming code in a processor firmware layer.
1	7. The method of claim 1 further comprising storing the
2	programming code in a non-volatile memory.

- 1 8. The method of claim 1 further comprising utilizing the first 2 register as an index register during execution of the programming code.
- 9. The method of claim 1 further comprising utilizing the first
 register as a predicate register during execution of the programming code.

1	10. The method of claim 1 further comprising saving rest of processor
2	states before execution of interrupt handlers.
1	11. A digital processing system comprising:
2	an execution unit;
3	a general purpose register file coupled to the execution unit
4	containing a plurality of general-purpose registers;
5	a memory coupled to the execution unit for storing a processor
6	abstraction layer, the processor abstraction layer further
7	including interrupt handlers, each of the interrupt handler
8	further including saving architecture state code, the saving
9	architecture state code further including a plurality of
10	predefined sections, wherein each the predefined section
11	corresponds to a logic value of a register whereby the logic
12	value can be restored in response to the predefined sections.
1	12. The digital processing system of claim 11, wherein the saving
2	architecture state code is stored in a non-volatile memory.
1	13. The digital processing system of claim 11, wherein the register is
2	multiple bits wide.
1	14. The digital processing system of claim 11, wherein the logic value
2	can be restored in the register.
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	1	19. The article of manufacture of claim 18, further including computer
	2	readable program code for:
` \	3	identifying a second logic value stored in a second register;
K/	4	branching to a second predefined location within the programming
	5	code in response to the second logic value;
	6	utilizing the second register as scratch register during execution of the
	7	programming code; and
	8	restoring the second logic value back to the second register in
	9	response to the second predefined location.
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	1	20. The article of manufacture of claim 18, wherein the branching to a
	2	first predefined location further including computer readable program code
	3	for identifying the first predefined location from a plurality of predefined
4e	4	locations in the programming code.
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Had Had Hink Arm Ham	1	21. The article of manufacture of claim 18, further including computer
	2	readable program code for executing the programming code in a processor
	3	firmware layer.

	1	22. A computer system comprising:
	2	means for identifying a first logic value stored in a first register;
. \	3	means for branching to a first predefined location within a
14	4	programming code based upon the first logic value;
1	5	means for utilizing the first register as a scratch register during
	6	execution of the programming code;
	7	means for restoring the first logic value back to the first register in
	8	response to the first predefined location.
F≅ş	1	23. The computer system of claim 22, further comprising means for
	2	detecting an occurrence of an interrupt during execution.
* #! * <u></u>		
17.20 RR HR 18.20 A. 18.20 B. 18.20 B. 18.20	1	24. The computer system of claim 22, further comprising:
	2	means for identifying a second logic value stored in a second register;
!	3	means for branching to a second predefined location within the
1 1 1 1 1 1 11	4	programming code in response to the second logic value;
	5	means for utilizing the second register as scratch register during
# # #	6	execution of the programming code;
	7	means for restoring the second logic value back to the second register
	8	in response to the second predefined location.



- 1 25. The computer system of claim 22, wherein the branching to a first
- 2 predefined location further including means for identifying the first
- 3 predefined location from a plurality of predefined locations in the
- 4 programming code
- 1 26. The computer system of claim 22, further comprising means for
- 2 executing the programming code in a processor firmware layer.
- 1 27. The computer system of claim 22, further comprising means for
- 2 storing the programming code in a non-volatile memory.
- 1 28. The computer system of claim 22, further comprising means for
- 2 utilizing the first register as an index register during execution of the
- 3 programming code.

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